



(19)

(11) Publication number: **2001**

Generated Document.

PATENT ABSTRACTS OF JAPAN(21) Application number: **2000004968**(51) Intl. Cl.: **H01L 21/288 H01L 21/3205**(22) Application date: **13.01.00**

(30) Priority:	14.01.99 US 99 231616	(71) Applicant: INTERNATL BUSINESS CORP <IBM>
(43) Date of application publication:	28.07.00	(72) Inventor: SAIPURAIAN E UZOO
(84) Designated contracting states:		(74) Representative:

**(54) VIA PLATING
METHOD, PRODUCTION
OF VIA PLATING
STRUCTURE AND
MULTILAYER
INTERCONNECTION
STRUCTURE**

(57) Abstract:

PROBLEM TO BE SOLVED: To reduce formation of a void when a via is filled by providing an electrically conductive interconnection in a via through electroplating in a bath containing an aliphatic amine alkoxylate surfactant.

SOLUTION: An undercut structural part can be obtained by etching an RIE mask 3 and an underlying polymer layer 2 sequentially. A barrier layer 5 is deposited on the structural part by means of CVD or electroless plating. In order to deposit a seed layer 6, Cu is deposited on the layer 5 by sputtering. A continuous structure 6 of the barrier layer 5 and the seed layer is formed by

10676208
10/29/03

combining the metal sputtering deposition and the metal sputtering etching well. The undercut part is filled by electrodeposition through electroplating bath containing a smoothing additive, and an alkanol ACN akiphatic amine alkoxylate based surfactant in an aqueous medium.

COPYRIGHT: (C)2000,JPO

